ABSTRACT

In a clock generation circuit generating a clock that is synchronized with a reference signal, it is an object to provide stable clocks by controlling phase jitter in a generated clock upon change of the reference signal, eliminate a stable-state phase difference between the reference signal and the generated clock so that control is eliminated, and allow the clock generation circuit to be integrated. The clock generation circuit is configured with multiple stages of PLL circuits such that PLL circuits 2 are provided for reference signals 1, respectively, and one of outputs from the PLL circuits 2 is selected to be fed to a PLL circuit 5 provided in a next stage. The phase fluctuation of a signal inputted to the PLL circuit 5 upon change of the reference signal 1 is reduced to control the phase jitter of the generated clock 6, thus allowing high loop gain in both the PLL circuit 2 and the PLL circuit 5. Then, phase difference between the reference signal 1 and the generated clock 6 is eliminated to eliminate control involved, so that the clock generation circuit may be integrated.